WHAT IS CLAIMED IS:

1. A method for modeling a semiconductor device process, comprising:

(a) setting data of an SiO_2 layer;

(b) setting data of an Si layer brought in contact with said SiO_2 layer;

(c) setting a plurality of cells in said Si layer, and setting an amount of an impurity included in each of said cells;

(d) setting an amount per unit time by which said impurity included in each of said cells moves to another cell;

(e) setting data by which said cell in the vicinity of an interface of said SiO_2 layer and said Si layer is set as an impurity pileup portion;

(f) setting data of a position of a source or a drain in said Si layer; and

(g) calculating the amount of said impurity included in each of said cells for each unit time after processing the steps (a)~(f),

wherein a mass of said impurity moving to said pileup portion from each of said cells is determined as a function of a distance to said impurity pileup portion from each of said cells (hereinafter referred to as a distance r1), and a distance to said source or said drain from each of said cells (hereinafter referred to as a distance r2).

2. The method for modeling the semiconductor device process according to claim 1 wherein the data of the position of said source or said drain is set so that said source or said drain is distributed in a predetermined region in said Si layer, and said distance r2 is a distance between each of said cells and said predetermined region.

3. The method for modeling the semiconductor device process according to claim 1 wherein the movement mass of said impurity is determined as a function of a solid angle considering each of said cells set as said impurity pileup portion from each of said cells.

4. The method for modeling the semiconductor device process according to claim 1, further comprising setting data in which a part of said impurity is generated or disappears for each unit time.

5. The method for modeling the semiconductor device process according to claim 1 wherein said step(f) comprises:

assuming that a plurality of said sources or said drains exist in said Si layer; and

setting data in which the data of the position of specified said source or the data of the position of specified said drain is ignored.

6. The method for modeling the semiconductor device process according to claim 1, further comprising: step(h) storing data of a magnitude of a reverse short channel effect; and a ninth step of using the impurity amount calculated by said step(g) to calculate a threshold voltage.

7. The method for modeling the semiconductor device process according to claim 1, further comprising a step of setting data of an insulating layer disposed opposite to said SiO_2 layer via said Si layer.